REMARKS

Claims 1, 9-17, 21, and 22 are presently active.

In the Office Action dated 12 February 2004 ("Office Action"), claims 9 and 10 were rejected under 35 U.S.C. §102(b) as being anticipated by Hariton, US patent 5,926,064 ("Hariton"); claims 11 and 12 were rejected under 35 U.S.C. §103(a) as being unpatentable over Hariton; claims 13-16 were rejected under 35 U.S.C. §103(a) as being unpatentable over Applicant's admitted prior art Fig. 2 in view of Hariton; and claims 1, 17, 21, and 22 were allowed.

Applicant acknowledges with appreciation the allowance of claims 1, 17, 21, and 22.

Applicant appreciates the Examiner's answer near the middle of page 5 of the Office Action to the question posed in the previous communication from the Applicant, where it is indicated in the Office Action that the claims should recite that the circuit elements are "directly" connected where necessary. Accordingly, claims 9, 11, and 13-16 are amended to better define and more particularly point out the invention by inserting "directly" before "connected".

It is believed that the claims are patentable over the cited references. Specifically, referring to Fig. 5 of Hariton, the gate of nMOSFET 505 is connected to the gate of nMOSFET 506 and the drain of nMOSFET 505. The drain of nMOSFET 505 is connected to the drain of pMOSFET 504. However, the gate and drain of nMOSFET 505 are not directly connected to the sources and drains of transistors 302 and 303. Therefore, the presently active claims are not anticipated or suggested by Hariton.

The other cited references were cited merely for teaching the use of a bipolar transistor in place of a FET, or for teaching the substitution of a floating capacitor for a generic capacitor in a communication device.

Accordingly, it is believed that the presently active claims are neither anticipated nor suggested by the cited references.

Respectfully submitted,

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